A 7 level Metallization with Cu Damascene Process using Newly Developed Abrasive Free Polishing

H. Yamaguchi, N. Ohashi, T. Imai, K. Torii, J. Noguchi, T.Fujiwara
T.Saito, N.Owada,*Y. Homma, *S. Kondo and *K. Hinode

Device Development Center, Hitachi, Ltd.,
6-16-3, Shin-machi, Ome-shi, Tokyo 198-8512, Japan
*Central Research Laboratory, Hitachi , Ltd.,
1-280 Higashi-Koigakubo, Kokubunji-shi, Tokyo 185-8601, Japan

Abstract

A 7 level metallization including 4 levels of Cu metallization by the damascene technique is successfully developed using newly developed abrasive free polishing(AFP). This new AFP process reduced erosion and dishing, defect density, and improved TDDB lifetime of dielectric layers. We also improved corrosion resistance for Cu wiring. This process was used to fabricate a metallization structure of a new-cache memory chip consisting of 9-Mb 0.6-ns SRAMs and 200-K 25ps ECL gate arrays. And this Cu metallization suppresses parasitic capacitance of interconnects and reduces clock wiring delay by 30%.

Introduction

A Cu damascene process is one of the most promising technologies to realize the Cu interconnection structures for high-speed logic LSIs(1). The key technologies for Cu damascene process include Cu filling into trenches and Cu CMP. As for the Cu deposition, various technologies have been studied to fill trenches and holes. Among these technologies, low pressure long throw sputtering combined with reflow process is one of the most promising and well established technologies.(2)(3) Once the deposition technology is fixed, CMP technology for Cu becomes almost the only one key process to establish Cu metallization.

As is well known, there exist many problems to be solved in Cu CMP process, including erosion, dishing, corrosion, particles generated from slurry, scratches, mechanical damage to the substrate, and so on. Before introducing Cu metallization process into mass production, these instabilities in Cu CMP process should be solved.

In this study, the advantage of a two step CMP process by using newly developed abrasive free polishing(AFP) for Cu is demonstrated and the successful application of this AFP technology to 7 level metallization including 4 levels of Cu layers is reported.

Experimental

After the CMOS and Bipolar transistors were fabricated on bonded SOI substrate, HDP(high density plasma) SiO_2 was deposited and CMP was carried out for premetal planarization. After contact holes were filled with tungsten plug and first level metallization was formed with the conventional subtractive method, Cu single damascene process with tungsten plug was performed from the metal 2 and metal 5. After the trench etching, Cu film was deposited by long throw sputtering with TiN barrier layer, which was followed by reflow of Cu film. Then metal removal by CMP and post CMP wet cleaning was performed using the newly developed AFP. Two step CMP process was used in which the first step was designed only for Cu CMP and the second step was to remove barrier layer. Then, 0.05μm cap-pSiN as a barrier material against Cu diffusion was deposited in series with accompanying NH3 plasma treatment to reduce CuO from the Cu surface.

Defects and Cu corrosion were evaluated using KLA2138 wafer inspection tool combined with Applied Materials review SEM. Time dependent dielectric breakdown (TDDB) between Cu interconnects in the same layer was measured at 140°C using a test structure consisting of comb lines capacitor. The lifetime is defined as the time at which the leakage current density exceeds $1\mu A/cm^2$.

Results and discussion

A. Two step Cu CMP process

As the newly developed AFP removes Cu only chemically, the selectivity of Cu polishing to the underlying TiN is almost infinite, and a complete stop-on-barrier characteristic is realized. Fig.1 shows the cross section of Cu interconnect, and it is shown that the TiN remains almost completely even after 50% over polishing of Cu. Next, making the best use of this characteristics, the TiN layer was polished by using an abrasive slurry having a controlled CMP selectivity of TiN against SiO_2 and Cu to minimize the erosion and dishing. Fig.2 shows the metal residues at the upper tungsten plug CMP process in case of adoption of AFP for the first CMP step, comparing the case of conventional abrasive slurry. In case of AFP process, we can eliminate the residue completely by the reduction of dishing and erosion, resulting in the improvement of the process window. Fig.3 shows the cross section of our 7 level metallization in which metal 2,3,4 and 5 were Cu damascene interconnects, showing the successful application of this AFP process. And this Cu metallization suppresses parasitic capacitance of interconnects and reduces clock wiring delay by 30%(4).

B. Corrosion inhibition

As Cu is the material to be corroded very easily, Cu CMP process should be designed so as to eliminate the Cu corrosion during the whole chemical treatment. In our study, serious corrosion problem was observed in the actual device wafers, in which so many PN junctions with various area are included, especially at the patterns connected to the special PN junctions. Fig.4 shows the relationship between PN junction area and photo induced current through the PN junctions together with the occurrence of Cu wiring corrosion. As is shown in this figure, photo induced current increases with the increase in PN junction area, and the corrosion is observed when the PN junction area exceeded $1.5x10^2(\mu m^2)$. The best way to eliminate this kind of corrosion is to completely eliminate photo irradiation from the

0-7803-6327-2/00/$10.00 © 2000 IEEE

environment. So our process was designed to completely shut out the photo irradiation through Cu CMP and post CMP wet cleaning. Fig.5 compares the effect of photo irradiation for the corroded pattern. (a) is with photo irradiation and (b) is without photo irradiation. As is clearly shown in this figure, the corrosion of Cu wiring pattern connected to the large PN junction area is completely suppressed by shutting the light out from the environment.

C. TDDB improvement

Fig.6 compares the TDDB lifetime between AFP(B) and conventional CMP(A). In this experiment, the case of special surface treatment with NH_3-plasma onto Cu interconnect was also shown(5). A commercially available abrasive slurry was used in the CMP(A). As is clearly shown in this figure, AFP(B) gives longer lifetime in both cases of with surface treatment and w/o treatment. In case of conventional CMP(A), the SiO_2 surface is likely to be severely damaged by the CMP process, resulting in dangling bond formation. On the other hand, in case of AFP, mechanical damage to the surface is expected to be reduced drastically. This reduction in the mechanical damage is supposed to contribute to longer lifetime in the newly developed AFP.

D. Defect reduction

As the abrasive free polishing solution does not include powders, particles and scratches induced by powder agglomeration can be eliminated completely. Table.1 shows the results of defect classification for the 18 wafers processed with this new AFP. Fig.7 also shows the examples of representative defects. As is clearly shown in these results, no scratches were detected and the killer defects detected by KLA2138 and review SEM were the simple defects in film deposition process and patterning process. As the defects level in this process does not include the special defects concerned with CMP process, the conventional yield management system works well even in this damascene process.

Conclusion

A 7 level metallization including 4 levels of Cu damascene wiring was successfully constructed using newly developed AFP. With this method, erosion and dishing were drastically reduced, and corrosion resistance was improved by shutting the photo irradiation from the environment. This new AFP was also very effective to improve TDDB lifetime supposedly because of mechanical damage reduction in the surface region of SiO_2. Defects such as scratches and particles induced by powder agglomeration was also reduced because of its inherent abrasive free characteristics. This kind of AFP is one of the most promising technology in the future Cu damascene process.

References

1)D.Edelstein, J.Heidenreich, R.Goldblatt, W.Cote, C.Uzoh, N.Lustig, P.Roper, T.McDevitt, W.Mostiff, A.Simon, J.Dukovic, R.Wachnik, H.Rathore, R.Schulz, L.Su, S.Luce and J.Slattery, in Technical Digest of International Electron Devices Meeting in 1997, pp.773-776, Washington, DC(1997).

2). T.Saito, N.Fukuda, H.Yamaguchi, S.Hirasawa, K.Hinode, and N.Owada, in Advanced Metallization and Interconnect Systems for ULSI Applications in 1996, edited by R.Havemann, J.Schmitz, H.Komiyama, and K.Tsubouchi (Mater. Res. Soc. Proc., Pittsburgh, PA, 1997) pp.149-154.

3)T.Saito, N.Ohashi, J.Yasuda, J. Noguchi, T. Imai, K.Sasajima, K.Hiruma, H.Yamaguchi and N.Owada, in proceedings of Interconnect Technology Conference in 1998, pp.160-162, San Francisco(1998).

4)T.Hashimoto, T.Kikuchi, K.Watanabe, N.Ohashi, T.Saito, H.Yamaguchi, S.Wada, N.Natsuaki, Y.Kondo, S.Kondo, Y.Homma, N.Owada and T.Ikeda, in Proceedings of 1998 IEDM, No 8-4, Sanfrancisco.

5)J.Noguchi, N.Ohashi, J.Yasuda, T.Jimbo, H.Yamaguchi, N.Owada, K.Takeda and K.Hinode, in Proceedings of IRPS 2000, to be published.

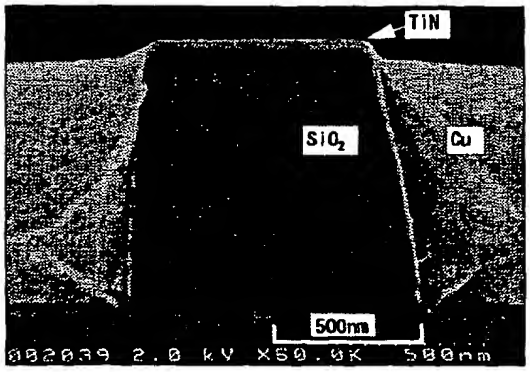
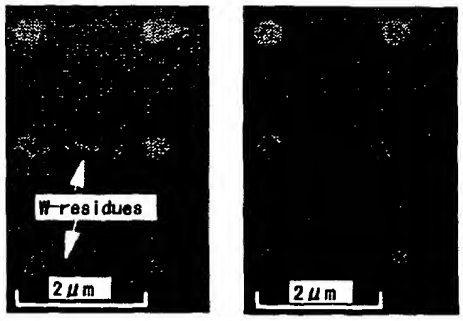


Fig.1 Cross section of Cu interconnect after the first CMP step.



(a) conventional abrasive CMP (b) AFP

Fig.2 Elimination of W-residues at the upper W-plug CMP process by adoption of AFP.

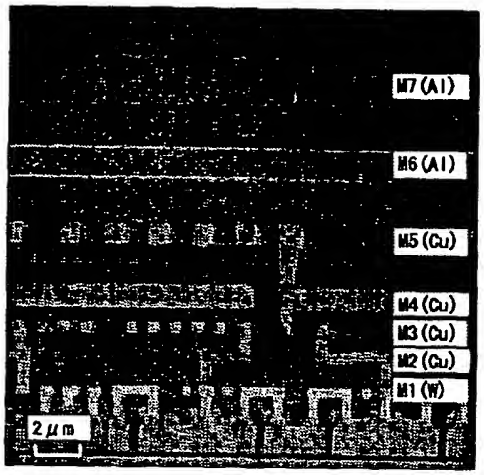


Fig.3 Cross section of the 7 level intercconection.

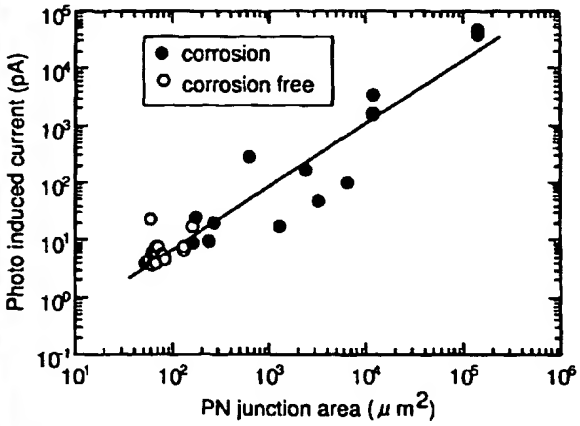
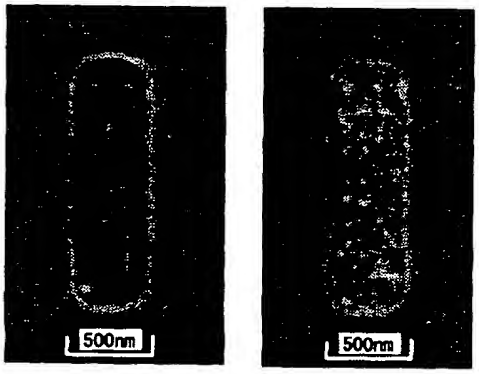


Fig.4 Relationship between PN junction area and photo induced current.



(a) with photo irradiation. (b) without photo irradiation.

Fig.5 Photo irradiation effect on Cu corrosion.

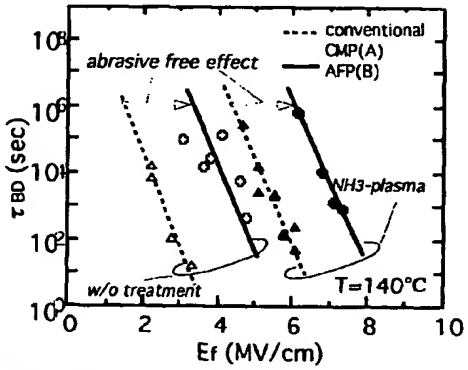
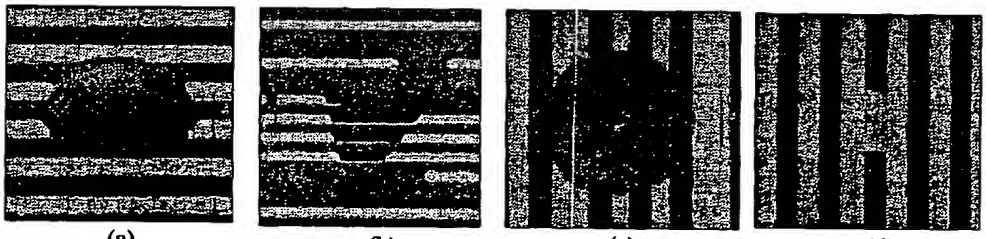


Fig.6 Effects of new CMP process and plasma treatment on life-time improvement .

Table.1 Results of defect classification for 18 wafers processed with abrasive free polishing(AFP).

Components	scratch	open			short	corrosion
		pattterning	others	dielectric particle		
defects/wafer	0	0.9	2.3	0.8	0.4	0
in Fig.7	-	(a)	(b)	(c)	(d)	-



(a) (b) (c) (d)

Fig.7 Examples of defects observed in Cu metallization with abrasive free polishing(AFP).